Jurnal Fisika Papua
Vol. 3, No. 2, Agustus 2024, pp. 64 - 70
e-ISSN: 2963-3702
DOI: 10.31957/jfp.v3i2.196

Model of Metal-Oxide-Semiconductor Contact Characteristics and Carrier Impurity Concentration in Depletion and Oxide Regions

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ABSTRACT

The aim of this research is to obtain characteristic modeling for forward and reverse voltage, the role of oxide as a barrier in contact between metal semiconductors. When a forward or reverse voltage is applied, both p and n types of semiconductors have different characteristics. In this research, only the p type is considered. The carrier concentration impurity within the semiconductor and the width of the oxide material, the depletion region and the active region are also reviewed. The method used is to examine the concept of metal-oxide-semiconductor contact. In addition, the basic concept of energy bands is used to explain carrier flow events in semiconductors which will present a band gap E_g, conduction band level E_C, and valence energy level E_V. The results of the first research are the characteristics of the metal – oxide – p type semiconductor connection when a negative (V<0) and positive (V>0) voltage is applied to the metal plate. The second is to find an equation to determine the concentration of the N_A substrate impurity. This equation can show how large the concentration of impurities is in the semiconductor and how wide the oxide material, depletion region and active region are.

Keywords: Metal-Oxide-Semiconductor Contact; Carrier Concentration.

1. Introduction

The metal-oxide-semiconductor (MOS) contact characteristics model is an important aspect in the development of modern semiconductor technology [1]. These contacts serve as an interface between the metal and semiconductor, greatly affecting the performance of electronic devices. In this context, understanding the concentration of impurity carriers in the depletion and oxide regions is crucial because it can influence the electrical properties and efficiency of the device. This research aims to develop a model that can explain the interaction between contact characteristics and impurity concentrations in these two regions [2][3].

The depletion region is the area around the semiconductor and oxide interface where the concentration of the majority carriers is reduced due to the influence of the electric field [4][5]. This phenomenon occurs when the gate voltage (VG) in an n-type semiconductor is less than zero, which causes a reduction in the donor (electron) concentration and formation of a carrier-free layer on the surface of the semiconductor. This has implications for changes in the current and capacitance characteristics of the MOS device; therefore, accurate modeling of this region is necessary to improve device performance [6].

On the other hand, the oxide region also plays an important role in the contact characteristics of MOS [7][8]. The oxide serves as a barrier separating the metal from the semiconductor, and the quality and thickness of the oxide can affect the charge-transfer efficiency. Impurities in the oxide can change the electrical properties, potentially increasing or decreasing device performance. Therefore, it is important to analyze how the impurity concentration in the oxide interacts with the existing electric field and influences the contact characteristics [9][10].

In this study, we use mathematical modeling and simulation approaches to explore the characteristics of metal-oxide-semiconductor contacts. By considering the influence of impurity concentrations in both regions, we hope that the resulting model can provide new insights into the dynamics that occur in MOS devices. The results of this research are expected to contribute to the development of more efficient and high-performance semiconductor technology [11][12]

In addition, this research also discusses how impurities can affect the carrier mobility in semiconductors. Carrier mobility is an important parameter that influences the conductivity of semiconductors, and is influenced by two types of resistance: lattice resistance (phonon scattering) and ionized impurity resistance [7]. By understanding this relationship, better devices can be designed by exploiting the unique properties of semiconductor materials [13].

Finally, this study aims to make a significant contribution to our understanding of the MOS contact characteristics and the influence of impurity

concentration. With a systematic and integrated approach, it is hoped that the results of this research can serve as a reference for further research and assist in future semiconductor technology innovations [15][16].

2. Method

The method used by the author in this research is a literature study that examines books related to the concept of metal-oxide-semiconductor contact. In addition, the basic concept of energy bands is used to explain carrier flow events in semiconductors. These energy bands represent the band gap E_g, conduction band level E_C, and valence energy level E_V.

2.1 Metal Oxide Semiconductor (MOS) Diodes

MOS diodes are the most important components of semiconductor physical devices because they are extremely useful in the study of semiconductor surfaces. In practical applications, the MOS diode is at the heart of the MOSFET, which is a very important device for IC integrated circuits. MOS diodes can also be used as storage capacitors in integrated circuits, which forms the basis for the development of building blocks for charge-coupled devices (CCDs). In this section, we review their characteristics in the ideal case and then expand the review to cover the effects of metal-semiconductor differences in work function, interfacial curvature, and oxide charges.

2.2 Working Principle of Ideal MOS Diode

A view of the MOS Diode is shown in Figure 1. A cross-section of the device is shown in Figure 2, where d is the thickness of the oxide and V is the applied voltage across the metal plate. In this section, we use the convention that the voltage V is positive when the metal plate is positively biased in contact with an ohmic contact, and V is negative when the metal plate is negatively biased in contact with an ohmic contact.

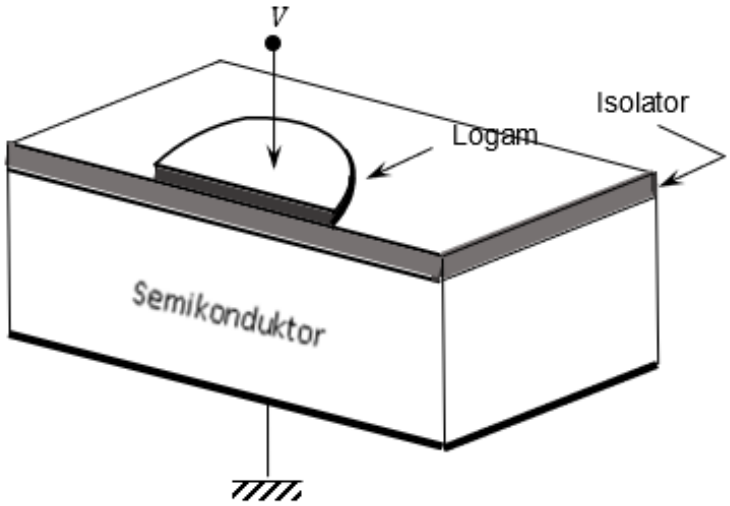

Figure 1. Perspective view of a metal oxide semiconductor (MOS) diode [17][18].

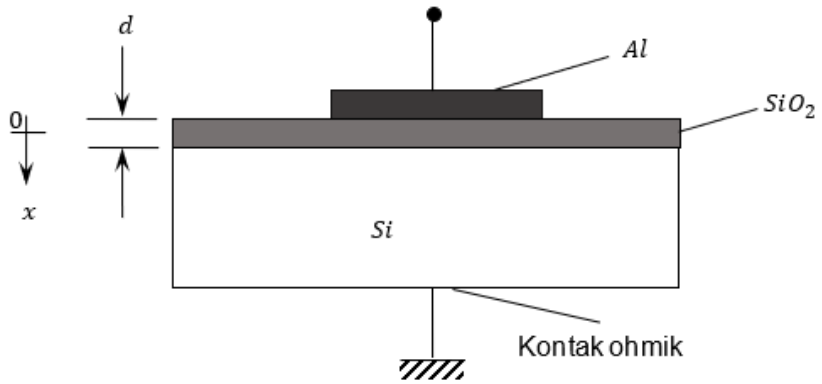

Figure 2. Cross section of MOS diode.

The energy band diagram of an ideal p-type MOS semiconductor at V=0 is shown in Figure 2. The work function is the energy difference between the Fermi level and vacuum level (i.e., $q\phi_m$ for metals and $q\phi_s$ for semiconductors). In addition, the electron affinities $q\chi$, which is the energy difference between the conduction

band eye and the vacuum level in the semiconductor, and $q\psi_B$, which is the energy difference between the Fermi level E_F and intrinsic Fermi level E_i.. An ideal MOS is defined as follows:

At an applied voltage, the energy difference between the metal work function $q\phi_m$ and semiconductor work function $q\phi_s$ is zero, or the work function difference $q\phi_{ms}$ is zero.

$$q\phi_{ms} \equiv (q\phi_m - q\phi_s) = q\phi_m - \left(q\chi + \frac{E_g}{2} + q\psi_B\right) = 0 \quad (1)$$

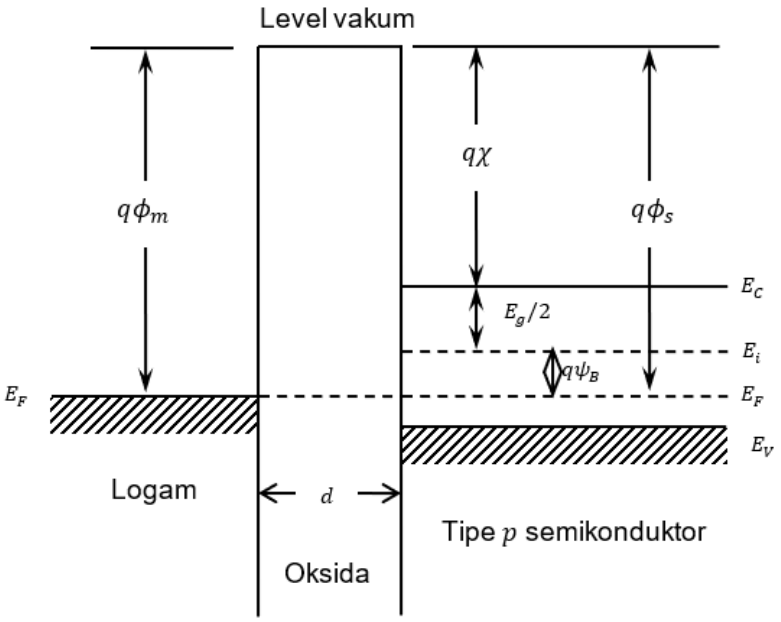

Figure 3. Energy band diagram of an ideal p-type MOS at V=0 [19]

where the sum of the three items in parentheses is equal to $q\phi_s$. In other words, the energy band is flat (plated band condition) when no voltage is applied. (b) Only the charges present in the diode under certain bias conditions are in the semiconductor and are of the same but opposite sign on the metal surface facing the oxide. (c) There is no carrier transport through an oxide under direct current (dc) – the bias condition–or the resistivity of the oxide is infinite. The MOS diode theory serves as a foundation for understanding practical MOS devices [20].

3. Results and Discussion

3.1 Applying Voltage to the MOS

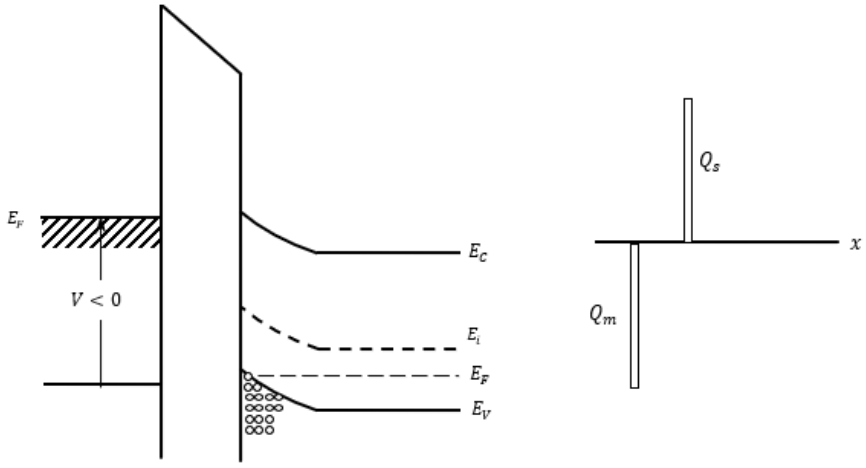

Figure 4. Case of p-type semiconductor, when a negative voltage (V<0) is applied to the metal plate

When an ideal MOS diode is applied with positive or negative voltage, three cases can occur on the semiconductor surface. In the case of p-type semiconductors, when a negative voltage (V<0) is applied to the metal plate, excess positive carriers (holes) are induced at the $SiO_2 - Si$ interface. In this case, the band near the surface of the semiconductor tends to increase, as shown in Figure 4. For an ideal MOS diode, no current flows in the device, regardless of the value of the applied voltage; therefore, the Fermi level in the semiconductor remains constant. Previously, we determined that the carrier density in a semiconductor depends exponentially on the energy difference $E_i - E_F$, that is,

$$p_p = n_i e^{(E_i - E_F)/kT} \quad (2)$$

The curved slope of the energy band at the semiconductor surface causes an increase in the $E_i - E_F$ energy there, which in return increases to a high concentration, the sum of holes near the semiconductor – oxide interface, which is called the accumulation case. The appropriate charge distribution is shown on the right side of Figure 5, where Q_s is the positive charge per unit area in the semiconductor and Q_m is the negative charge per unit area ($|Q_m| = Q_s$) in the metal [21].

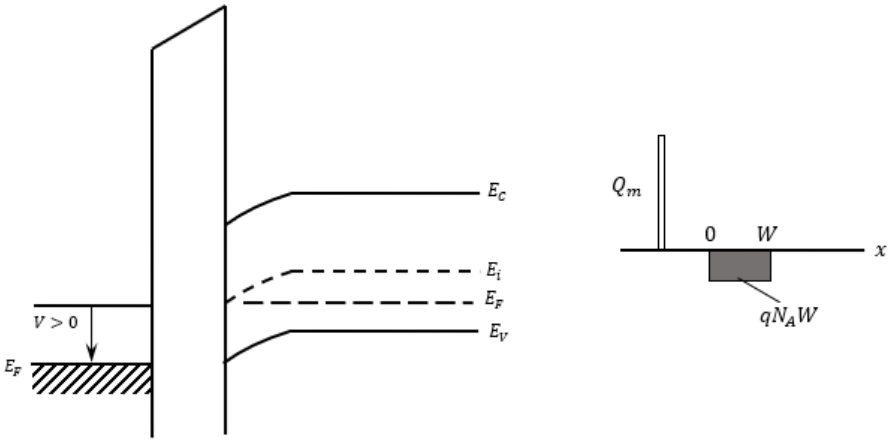

Figure 5. For the case of p-type semiconductor, when a negative voltage (V<0) is applied to the metal plate,

When a small positive voltage (V>0) is applied to an ideal MOS diode, the energy band near the surface of the semiconductor bends downward, and the majority carriers (holes) are evacuated (Figure 5). This is called the depletion case. The space charge per unit area Q_s, in a semiconductor is equal to $-qN_AW$, where W is the width of the surface of the depletion region.

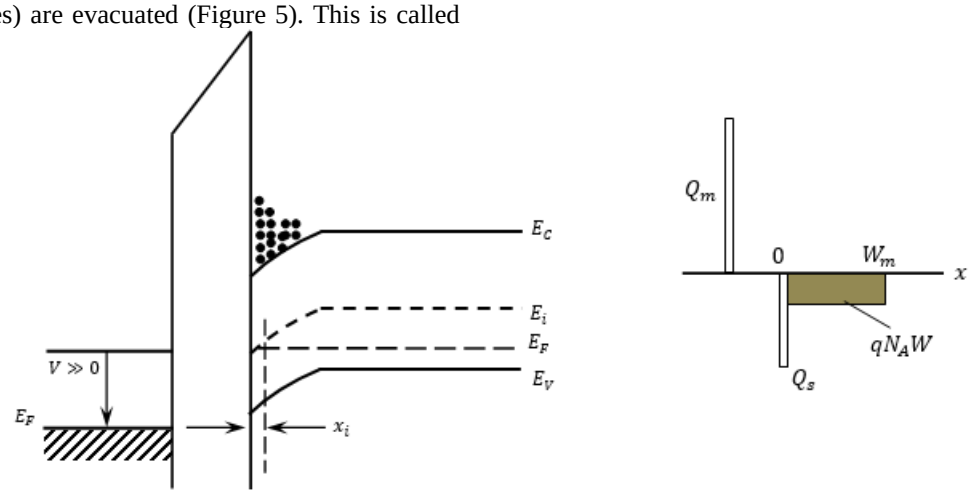

Figure 6. When a larger voltage is applied, the energy band bends downward, even more so that the intrinsic level $E_i$on the surface crosses past the Fermi level.

When a larger voltage is applied, the energy band curves downward, even more so that the intrinsic level E_i on the surface crosses past the Fermi level, as shown in Figure 6. In other words, a positive gate voltage begins to induce excess negative carriers (electrons). electrons) at the $SiO_2 - Si$ interface. The concentration of electrons

in a semiconductor depends exponentially on the energy difference $E_F - E_i$ and is given by

$$n_p = n_i e^{(E_F - E_i)/kT} \quad (3)$$

In the case shown in Figure 5, $(E_F - E_i) > 0$. Therefore, the electron concentration n_p at the interface becomes greater than n_i, and the hole concentration given by Equation (2) is less than n_i. The number of electrons (minority carriers) on the surface is greater than the number of holes (majority carriers); thus, the surface is inverted. This is known as the inversion case.

Initially, the surface was in a weak inversion state because the electron concentration was low. As the band bends further, the edge of the conduction band soon approaches the Fermi level. Initially, a strong inversion occurred when the electron concentration approached the $SiO_2 - Si$ interface equal to the substrate doping level. After this point, the bulk of the additional negative charge in the semiconductor consists of charge Q_n (Figure 6) in a very narrow$0 \le x \le x_i$ n-type inversion layer, where x_i is the width of the inversion region. Typically, the $x_i$values range from 1 to 10 nm and are always smaller than the surface width of the depletion layer.

Once strong inversion occurs, the surface width of the depletion layer reaches a maximum value. This is because when the band tends to decrease sufficiently for strong inversion to occur, even a small increase in the band curvature corresponding to a very small increase in the width of the depletion layer results in a large increase in the charge Q_n of the inversion layer. Therefore, under an inversion condition, the charge strength per unit area Q_s in the semiconductor is the sum of charge Q_n in the inversion layer and charge Q_sc in the depletion region.

$$Q_s = Q_n + Q_{sc} = Q_n - qN_A W_m \quad (4)$$

where $W_m$is the maximum width of the surface of the depletion region.

3.2 Surface Area Depletion Area

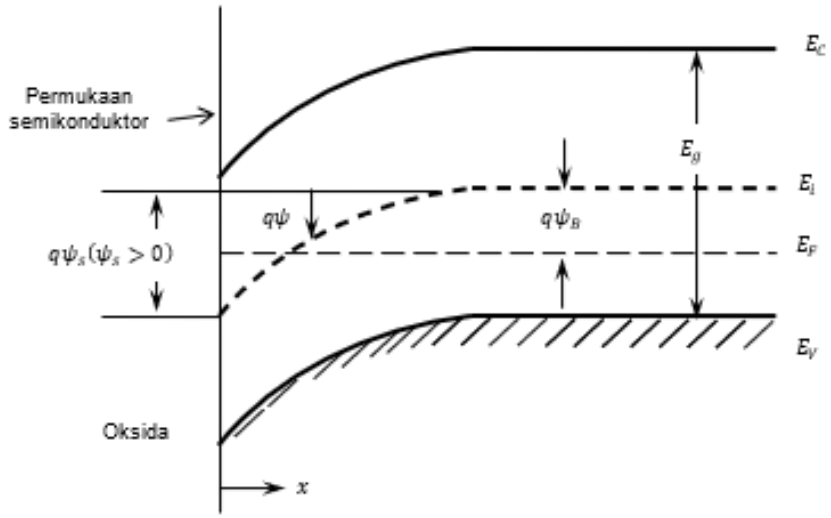

Figure 7. Band diagram on the surface of a p-type semiconductor where the electrostatic potential ψ is set as zero in the semiconductor bulk, at the surface of the semiconductor, $\psi = \psi_s$ is called the surface potential.

Figure 7 shows in more detail the band diagram on the surface of a p-type semiconductor. The electrostatic potential ψ is set to zero in the semiconductor bulk. On a semiconductor surface, $\psi = \psi_s$ is called the surface potential. We can express the hole and electron concentrations in equations (2) and (3) as a function of ψ:

$$n_p = n_i e^{(\psi - \psi_B)/kT} \quad (5a)$$
$$p_p = n_i e^{(\psi_B - \psi)/kT} \quad (5b)$$

where ψ is positive when the ribbon curves downward, as shown in Figure 7. At the surface the density is

$$n_s = n_i e^{(\psi_s - \psi_B)/kT} \quad (6a)$$
$$p_s = n_i e^{(\psi_B - \psi_s)/kT} \quad (6b)$$

From this discussion and with the help of equation (6), the following regions of the potential surface can be distinguished:
$\psi_s < 0$: Number of holes (upward curved ribbon).
$\psi_s = 0$: Flat band condition.
$\psi_B > \psi_s > 0$: Depletion of holes (band curved downwards).
$\psi_s = \psi_B$: Midgap with $n_s = n_p = n_i$ (intrinsic concentration).
$\psi_s > \psi_B$: Invection (band curved downwards).

The potential ψ as a function of distance can be obtained using the one-dimensional Poisson equation:

$$\frac{d^2\psi}{dx^2} = \frac{-\rho_s(x)}{\varepsilon_s} \quad (7)$$

where $\rho_s(x)$ is the charge density per unit volume at position x and ε_s is the dielectric permittivity. We use the depletion approach because we have worked in the study of $p-n$ junctions. When the semiconductor is discharged to a width W and the joint charge within the semiconductor is given by $\rho_s = -qN_A$, integration of the Poisson equation gives the electrostatic potential distribution as a function of the distance x within a surface of the depletion region.

$$\psi = \psi_s \left(1 - \frac{x}{W}\right)^2 \quad (8)$$

The surface potential ψ_s is

$$\psi_s = \frac{qN_A W^2}{2\varepsilon_s} \quad (9)$$

Note that the potential distribution is identical to that for one side of the p-n junction plane.

The surface is inverted whenever ψ_s is greater than ψ_B. However, we require a benchmark for the onset of reversal, after which the charges on the reversal layer become significant. A simple rule of thumb is that the electron concentration at the surface is equal to the impurity concentration of the substrate, that is$n_s = N_A$. Since $N_A = n_i e^{q\psi_B/kT}$, from equation (5a) we get

$$\psi_s(\text{inv}) \cong 2\psi_B = \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right) \quad (10)$$

Equation (9) specifies that a potential ψ_B is required to curve the energy bands downward to the intrinsic state on the surface $(E_i = E_F)$, and the bands must then be curved downward by another $q\psi_B$ on the surface to obtain a strong inversion state.

As previously discussed, the surface depletion layer reaches its maximum when the surface is strongly overturned. Accordingly, the maximum width of the surface of the depletion region W_m is given by expression (9) in which ψ_s is equal to $\psi_s(\text{inv})$, or

$$W_m = \sqrt{\frac{2\varepsilon_s\psi_s(\text{inv})}{qN_A}} \cong \sqrt{\frac{2\varepsilon_s(2\psi_B)}{qN_A}} \quad (11)$$

atau

$$W_m = 2\sqrt{\frac{\varepsilon_s kT\ln\left(\frac{N_A}{n_i}\right)}{q^2 N_A}} \quad (12a)$$

dan

$$Q_{sc} = -qN_A W_m \cong -\sqrt{2q\varepsilon_s N_A(2\psi_B)} \quad (12b)$$

4. Conclusions and Recommendations

Conclusions

The contact between the metal oxide and semiconductor is arranged in energy bands, where the Fermi level is located between two materials (semiconductor and metal) that are different, both p- and n-type, with a distant junction. For each type of semiconductor, the reverse and forward voltages have different meanings. Oxides act as insulators, connecting two materials (metals and semiconductors). For p-type semiconductors, for example, when the inverse voltage is large, carrier impurities move from the semiconductor to the metal. However, if the inverse voltage is not too large, then carrier impurities will be in the depletion and oxide areas.

The carrier impurity concentration is implicit in equation (10), which shows how large the impurity concentration is in the semiconductor and the width of the oxide material, depletion region, and active region are. The formula for determining the impurity concentration N_A depends on the experimentally determined data, where the variables are potential ψ_B, dielectric permittivityε_s, and maximum surface width of the depletion region W_m.

Recommendation

Because this research is conceptual in nature, it is necessary to carry out other computational studies to calculate the concentration of carrier impurities in the oxide material, depletion region, and active region. An MOS application can be created from the data calculated by computing. Based on this, the author hopes that a MOSFET can be made, which, among other things, has an important role in the application of advanced technology, namely IC integrated circuits and nanotechnology devices.

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